Report

Digital Circuits WiSo 14/15

Lab 1

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# Part 1: SSI-Logic implementation of a Boolean Logic Equation with NAND2 gates

The aim of this lab experiment is to develop and test a digital circuit for a settling tank in which solids are separated from a liquid. During the experiment only the circuit for the inlet pump (P1) was realized as per the instructions of the guiding professor. The control of P1 depends on the input of one opacity sensor (S1) and two fill level sensors, measuring the liquid level in the middle of the tank and at the 90percents (L and U respectively). The logic of the P1 control s expressed by the Boolean expression given in the preparation: P1 = ¬U ˄ (S1 ˅ ¬L ).

The realized circuit consisted of two CMOS NAND2 gates (devices of type 7400), switch and voltage supply, and a multimeter for measuring the results. The input DC voltage (Vcc) was 5V. The switch was used to mimic the sensor outputs. The schematics for the circuit are given at Figure 1.

The results of the experiment were consistent with the prepared truth table and are as shown on Table 1, where the values of P1 from the preparation correspond to the Vout values.

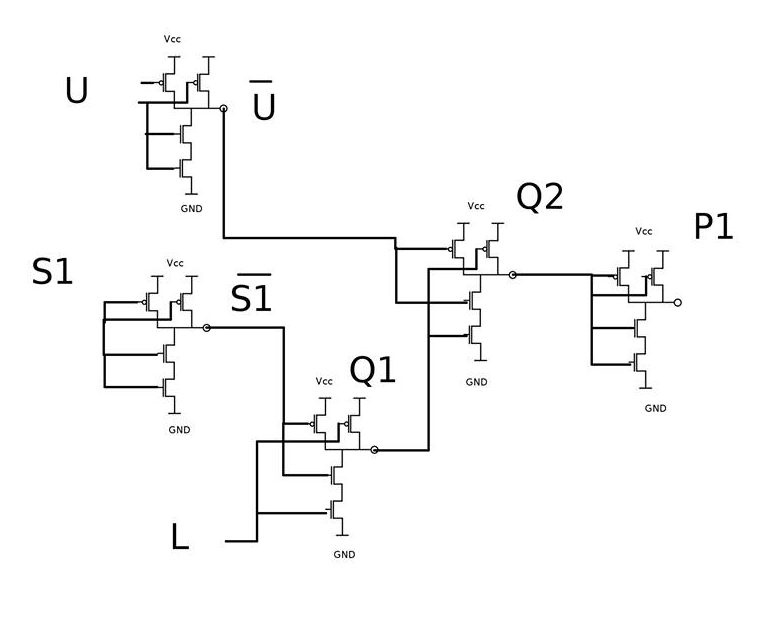


Figure 1. Schematics

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| U | L | S1 | P1 | Vout |
| 0 | **0** | **0** | **1** | **5,020V** |
| 0 | **0** | **1** | **1** | **5,020V** |
| 0 | **1** | **0** | **0** | **0.00V** |
| 0 | **1** | **1** | **1** | **5,020V** |
| 1 | **0** | **0** | **0** | **0.00V** |
| 1 | **0** | **1** | **0** | **0.00V** |
| 1 | **1** | **0** | **0** | **0.00V** |
| 1 | **1** | **1** | **0** | **0.00V** |

Table 1. Results from experiment 1

# Part 2: Measurement of the propagation delay of digital devices

The objective of the following two tasks is to show the propagation delay in of a CMOS inverter. The propagation delay is defined as the delay between a change in the input and the corresponding change in the output and is measured as 50% percent of the falling/rising wave (NPTEL). Figure 1 shows the graphical representation of the propagation delay measurement.

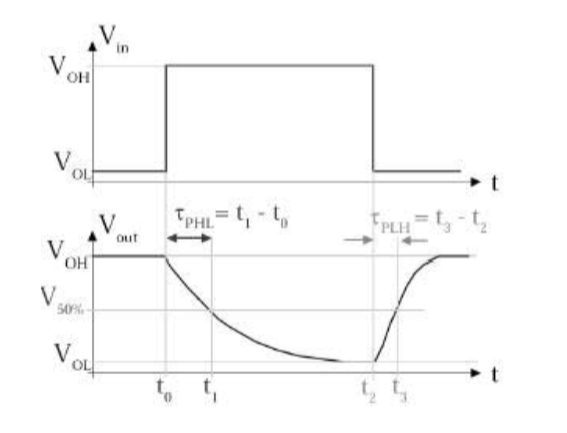


Figure 2. Measurement of propagation delay (NPTEL).

## Task 2.1

The propagation delay of the circuit from task 1 was measured when a rectangular wave with frequency *f*=1MHz was applied. The second input of the NAND2 gate was connected to GND so that the output varied with every change in the input.

The wave signal was connected to Chanel 1 of the oscilloscope and the NAND2 gate output – to Channel 2.

The following results were obtained:

* Propagation delay from High-to-Low – equals 32.100 ns (Figure 2);
* Propagation delay from Low-to-High – equals 30.00 ns (Figure 3).
* Total propagation delay for one gate = (τPHL + τPLH )/2 = 31.5ns

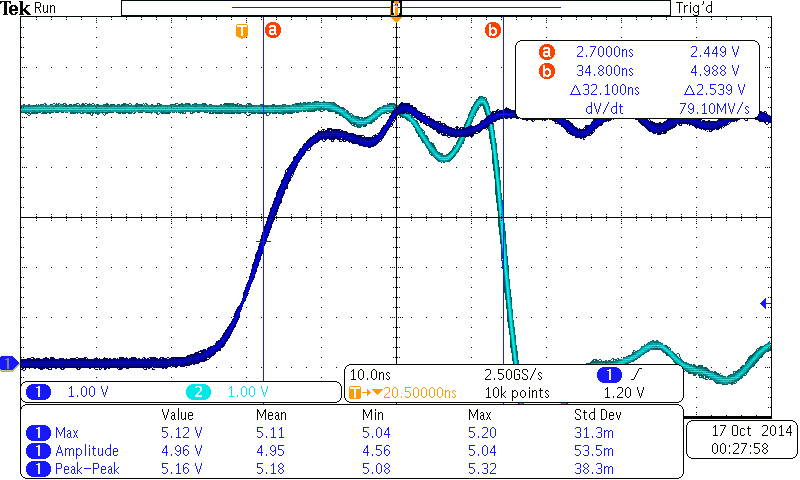


Figure 3. Propagation delay HL

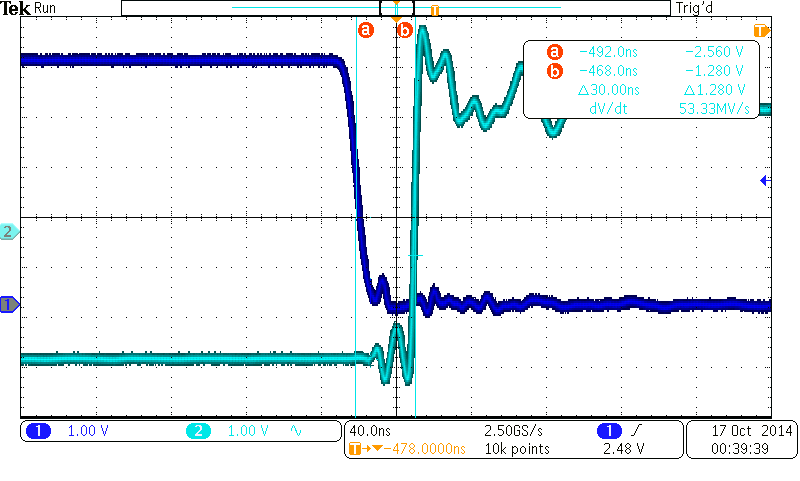


Figure 4. Propagation delay LH

## Task 2.2

During task 2.2 an overall delay of the signal of around 53.00ns was observed. This result together with the data from data sheet of the 74HC00 device (according to it the propagation delay of one NAND gate is between 10 ns and 15 ns (NXP, 2011)) leads to inconsistency.

# Task 3: Combinational loops

## Task 3.1

The aim of this task is to show the effects of improperly inserted feedback loops in digital circuits. A 74HC00 device with four NAND gates was used for the creation of the circuit on Figure 5. It has to be noted that the switch in Figure 5 is set up to GND.

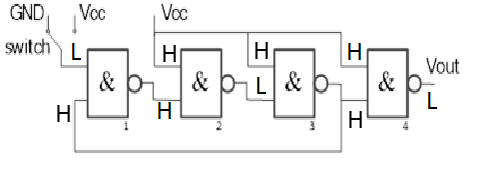


Figure 5. Combinational circuit with feedback loop

However, if the output is connected to Vcc the output of the circuit changes and this results in oscillations. The two cases are shown in Figure 6 and Figure 7 respectively.

The frequency of the wave was *f=*18.64MHz or period of 53.4ns. This is consistent with the results obtained from experiment 2.2 and lead to the conclusion the propagation delay for four NAND2 gates with a feedback loop is similar for that of five NAND2 gates.

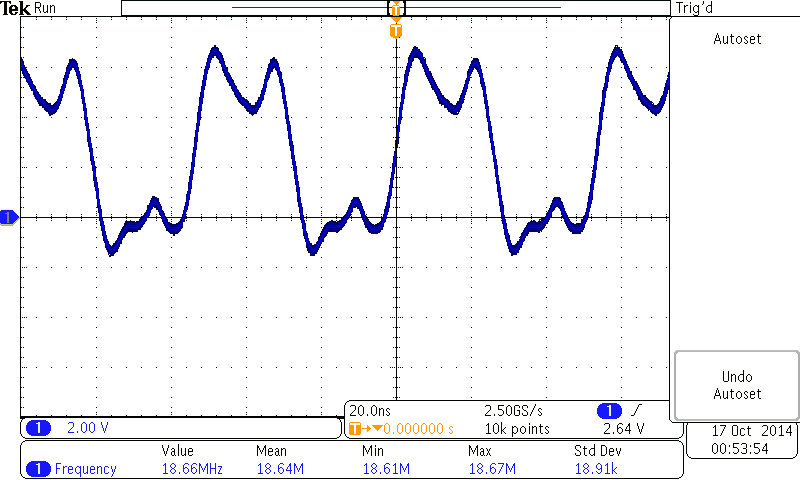


Figure 6. Combinational circuit output wave with switch at GND position

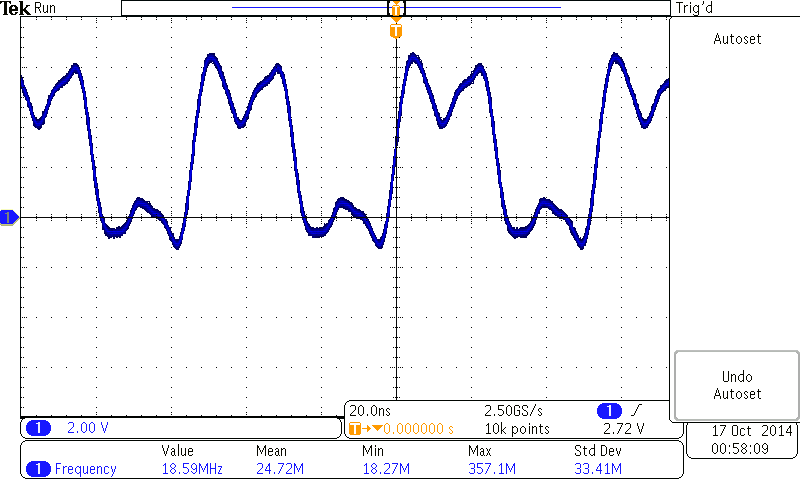


Figure 7. Combinational circuit output wave with switch at Vcc position

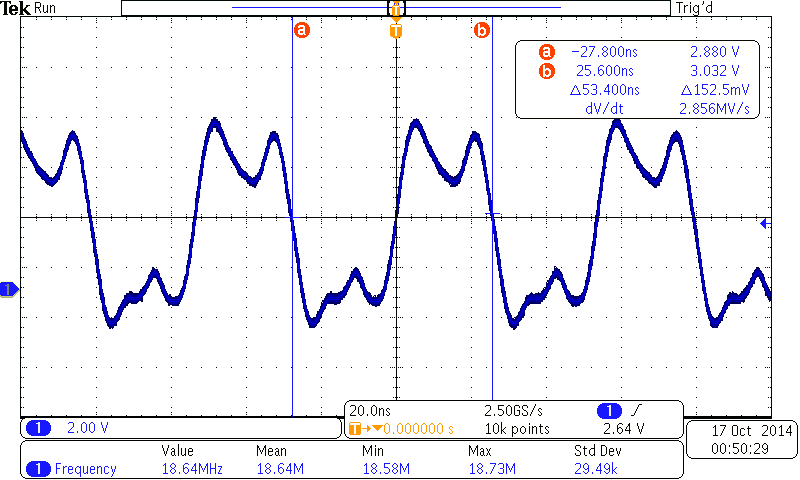


Figure 8. Period of Combinational logic circuit with feedback

# Part 4: Sequential circuit

## Task 4.1

The aim of this task is to display the behaviour of the signals from the sequential circuit in Figure 9 and to compare it with the preparation (Figure 11).

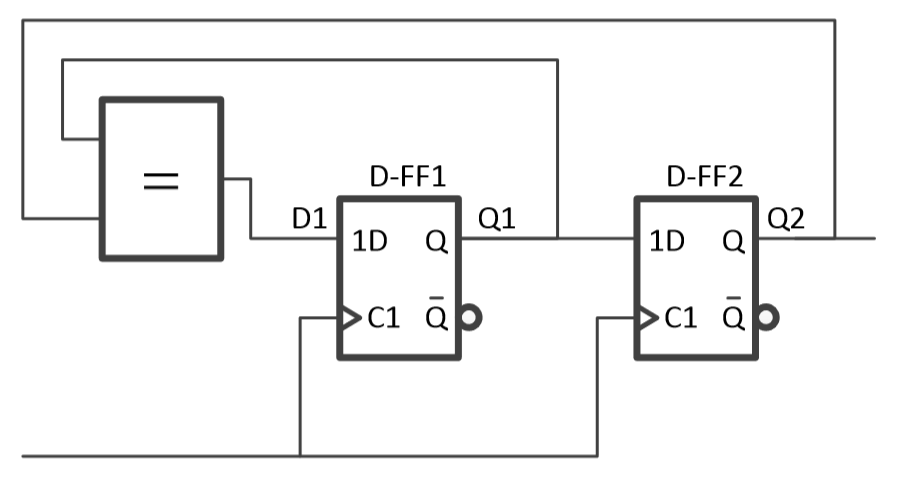


Figure 9. Sequential circuit without data inputs

At *f*=1MHz the behavior of the circuit is shown on Figure 10.

The signals are connected as follows:

* Channel 1 – CLK;
* Channel 2 – Q1;
* Channel 3 – Q2;
* Channel 4 – D1.

As it is easily seen the circuit behaves as expected.

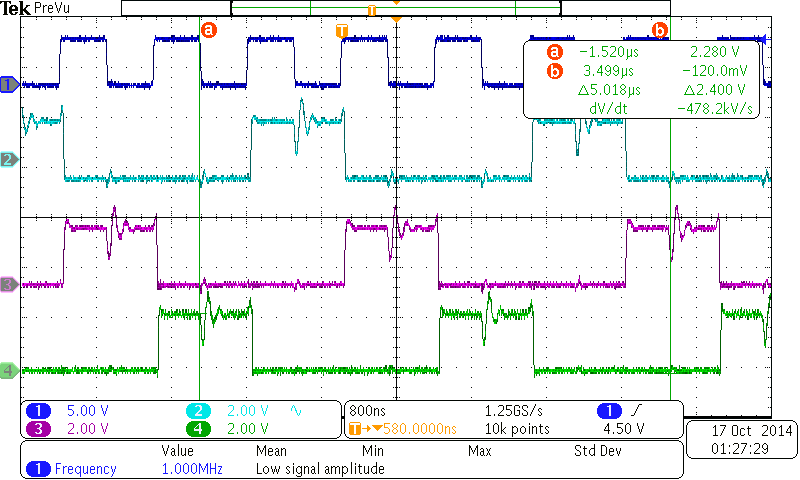


Figure 10. Sequential circuit output at f=1MHz

Figure . Preparation for task 4.1



The change of the output of the flop-flop happened 2.72µs after the first rising edge of the clock and the 5 periods of the clock were equal to 5.02µs.

## Extra task

For the extra task the same configuration as in Task 4.1 was used. After changing the frequency of the clock to higher frequencies, the wave forms were distorted and there were more oscillations. At *f*=5.195MHz the wave forms were still visible (Figure 12), however, at *f*=5.328MHz he signal lost the sequential pattern observed up to this specified limit (Figure 13).

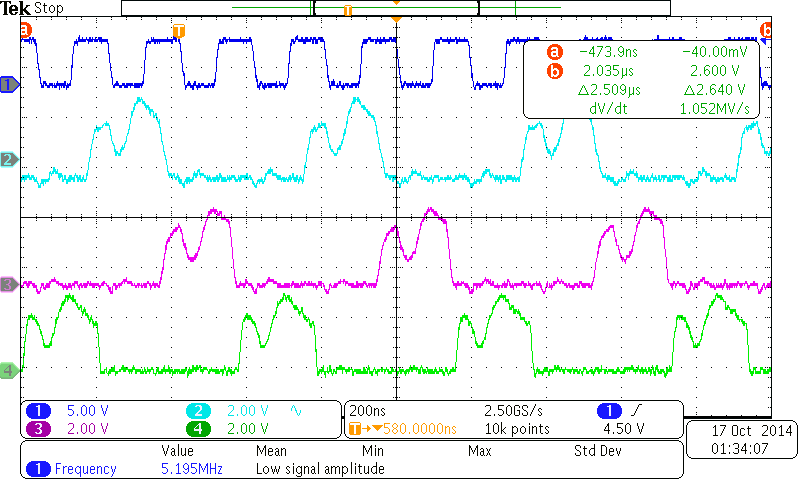


Figure 12. Wave forms at f=5.195MHz

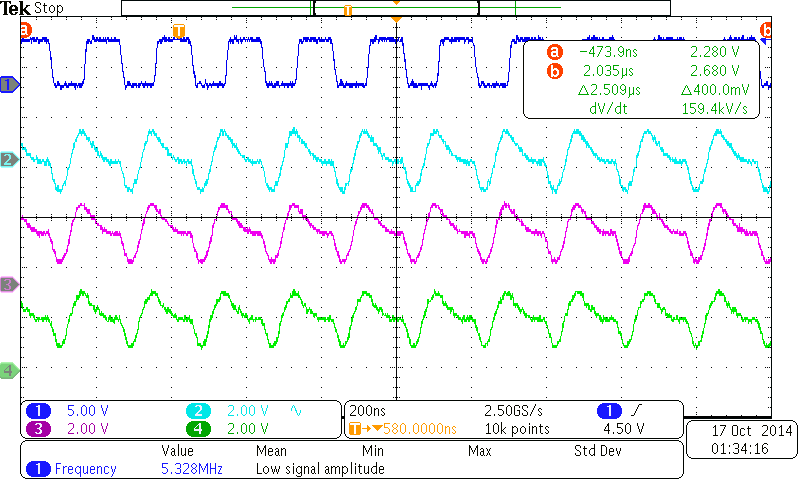


Figure 13. Wave forms at f=5.328MHz

# Conclusion

The experiment from Part 1 involved the creation of a controller and the results were consistent with the preparation and confirmed the validity of the truth table for the Pump1 of the settling tank controller.

Part 2 was designed to verify the theory behind the propagation delay measurement and gave some unexpected results, further investigation of the reasons for the results of task 2.1 would be beneficial.

Part 3 displayed the negative effects of unintentionally or improperly inserted feedback loops in a digital circuit. The results showed oscillations in the event of mishandling of the feedback loop.

Part 4 visualised the delay between clock signal and output of a digital circuit. The extra task set up an upper limit for the clock frequency at around 5MHz, above which the propagation delay influenced the signals too much and the digital circuit did not function properly.

# Bibliography

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